In the Claims

1. (Currently Amended) A method for receiving a DS-CDMA signal having in-phase and quadrature component waveforms each modulated by a pseudo-noise code of length M chips so that M chips, with each chip of the M chips having one or more data samples that are each comprised of one or more quantized bits, represent one information bit, said method comprising:

converting said in-phase component waveform into a first sequence of data samples;

converting said quadrature component waveform into a second sequence data samples;

selecting one or more data samples of each of the M chips and one or more quantized bits from each selected data sample from the first or second sequence of data samples to obtain a data sequence;

processing said data sequence to determine if a signal is present in the DS-CDMA signal; and if a signal is present:

collecting a predetermined number of samples from said first and second sequences of data samples; and

decoding a predetermined number of samples from said first and second sequences of data samples to recover information from the DS-CDMA signal;

wherein said first and second sequences of data samples are stored continuously in a circular buffer until a signal is detected in the DS-CDMA signal and a predetermined number of samples from said first and second sequences of data samples have been collected.

~~wherein each sample of said first and second sequence of data samples has a resolution of less than or equal to 10 bits~~.

2. (Original) A method as in claim 1, wherein said processing said data sequence to determine if a signal is present comprises:

coherently averaging said data sequence over one or more information bits to obtain an averaged data sequence of length M chips;

correlating said averaged data sequence with a pseudo-noise code sequence of length M to obtain a correlation output; and

comparing said correlation output with a predetermined threshold level to determine if a signal is present in the DS-CDMA signal.

3. (Original) A method as in claim 2, wherein the n^{th} element of said data sequence is denoted by c(n) and wherein said coherently averaging comprises:

calculating the sums $\sum_{p=0}^{P-1} c(k + M \cdot S \cdot p)$, wherein P is the number of averages, S is the number of samples per chip, M is the number of chips per information bit, k is the remainder portion of n/(MS) and p is the integer portion of n/(MS); and

quantizing each sum to the one or more quantized bits.

4. (Original) A method as in claim 3, wherein the number of averages, P, is equal to or less than 30.

5. (Original) A method as in claim 2, wherein said correlating said averaged data sequence with a pseudo-noise code comprises;

storing said averaged data sequence as a data bit pattern;

storing said pseudo-noise sequence as a pseudo-noise bit pattern;

performing a bit-wise "exclusive-or" operation between said data bit pattern and said pseudo-noise bit pattern; and

calculating, from the result of said "exclusive-or" operation, the number of bits that match between said data bit pattern and said pseudo-noise bit pattern.

6. (Original) A method as in claim 5, wherein said calculating from the result of said "exclusive-or" operation the number of bits that match between said data bit pattern and said pseudo-noise bit pattern is performed by use of a lookup table.

7. (Currently Amended) A method as in claim 1, wherein said converting said in-phase component waveform into a first sequence of data samples and said converting said quadrature component waveform into a second sequence of data samples are performed by first and second analog-to-digital converters.

8. (Original) A method as in claim 1, wherein said converting said in-phase component waveform into a first sequence of data samples and said converting said quadrature component waveform into a second sequence data samples are performed by a two-into-one multiplexer followed by an analog-to-digital converter.

9. (Cancelled)

10. (Original) A method as in claim 1, wherein said in-phase and quadrature waveforms are sampled at a rate of XRc, wherein Rc is the chip rate in the DS-CDMA signal and X is the number of samples per chip.

11. (Cancelled)

12. (Original) A method as in claim 1, wherein said first and second sequences of data samples are multiplexed together, packed into x8-bit words and passed to a processor for decoding.

13. (Original) A method as in claim 1, wherein said processing said data sequence to determine is a signal is present in the DS-CDMA signal and said decoding a predetermined number of samples from said first and second sequences of data samples to recover information from the DS-CDMA signal is performed on a digital signal processor.

14. (Original) A method as in claim 1, wherein said decoding comprises:

correlating said predetermined number of samples from said first and second sequences of data samples with a pseudo-noise sequence to obtain a plurality of correlation values; and

determining the information in the DS-CDMA signal from said plurality of correlation values.

15. (Original) A method as in claim 1, wherein said selecting includes sub-sampling said first or second sequence data samples to a rate of one sample per chip.

16. (Original) A computer readable medium containing instructions which, when executed on a computer, carry out a process of receiving a sampled DS-CDMA signal, said process comprising:

causing one or more data samples of each of M chips and one or more quantized bits from each selected data sample of the sampled DS-CDMA signal to be stored in a first memory as a data sequence, said data sequence being representative of an in-phase or quadrature component of the sampled DS-CDMA signal;

retrieving said data sequence from said first memory;

processing said data sequence to determine if a signal is present in the DS-CDMA signal; and if a signal is present:

causing a predetermined number of samples of the DS-CDMA signal to be stored in a second memory;

retrieving said predetermined number of samples of the sampled DS-CDMA signal from said second memory; and

decoding said predetermined number of samples of the sampled DS-CDMA signal to recover information from the sampled DS-CDMA signal.

17. (Original) A computer readable medium containing instructions as in claim 16, wherein said processing said data sequence to determine is a signal is present comprises:

coherently averaging said data sequence over one or more information bits to obtain an averaged data sequence of length M;

correlating said averaged data sequence with a pseudo-noise code of length M samples to obtain a correlation output; and

comparing said correlation output with a predetermined threshold level to determine if a signal is present in the DS-CDMA signal.

18. (Original) A computer readable medium containing instructions as in claim 17, wherein the n^{th} element of said data sequence is denoted by c(n) and wherein said coherently averaging comprises:

calculating the sums $\sum_{p=0}^{P-1} c(k + M \cdot S \cdot p)$, wherein P is the number of averages, S is the number of samples per chip, M is the number of chips per information bit, k is the remainder portion of n/(MS) and p is the integer portion of n/(MS); and

quantizing each sum to the one or more quantized bits of each selected data sample.

19. (Original) A computer readable medium containing instructions as in claim 17, wherein said correlating said averaged data sequence with a pseudo-noise code comprises;

storing said averaged data sequence as a data bit pattern;

storing said pseudo-noise sequence as a pseudo-noise bit pattern;

performing a bit-wise "exclusive-or" operation between said data bit pattern and said pseudo-noise bit pattern; and

calculating, from the result of said "exclusive-or" operation, the number of bits that match between said data bit pattern and said pseudo-noise bit pattern.

20. (Original) A device for processing a sampled DS-CDMA signal, wherein the device is directed by a computer program that is embedded in at least one of:

(a) a memory;

(b) an application specific integrated circuit;

(c) a digital signal processor; and

(d) a field programmable gate array, and the computer program, when executed, carries out the process of:

causing a plurality of data samples of each of M chips and a plurality of quantized bits from each selected data sample of the sampled DS-CDMA signal to be stored in a first memory as a data sequence, said data sequence being representative of an in-phase or quadrature component of the sampled DS-CDMA signal;

retrieving said data sequence from said first memory;

processing said data sequence to determine if a signal is present in the sampled DS-CDMA signal; and if a signal is present:

causing a predetermined number of samples of the sampled DS-CDMA signal to be stored in a second memory;

retrieving said predetermined number of samples of the sampled DS-CDMA signal from said second memory; and

decoding a predetermined number of samples of the sampled DS-CDMA signal to recover information from the sampled DS-CDMA signal.

21. (Original) A device for processing a sampled DS-CDMA signal as in claim 20, wherein said sampled DS-CDMA signal has in-phase and quadrature components, said device further comprising:

a first analog to digital converter for receiving an in-phase component of a DS-CDMA waveform and producing the in-phase component of the sampled DS-CDMA signal; and

a second analog to digital converter for receiving a quadrature component of a DS-CDMA waveform and producing the quadrature component of the sampled DS-CDMA signal.

22. (Original) A device for processing a sampled DS-CDMA signal as in claim 21, further comprising:

a means for extracting a plurality of data samples of each of the M chips and a plurality of quantized bits from each selected data sample of said in-phase or quadrature component of the sampled DS-CDMA signal to produce said data stream.

23. (Original) A device for processing a sampled DS-CDMA signal as in claim 20, wherein said processing said data sequence to determine is a signal is present comprises:

coherently averaging said data sequence over one or more information bits to obtain an averaged data sequence of length M;

correlating said averaged data sequence with a pseudo-noise code to obtain a correlation output; and

comparing said correlation output with a predetermined threshold level to determine is signal is present in the DS-CDMA signal.

24. (Original) A device for processing a sampled DS-CDMA signal as in claim 23, wherein the n^{th} element of said data sequence is denoted by c(n) and wherein said coherently averaging comprises:

calculating the sums $\sum_{p=0}^{P-1} c(k + M \cdot S \cdot p)$, wherein P is the number of averages, S is the number of samples per chip, M is the number of chips per information bit, k is the remainder portion of n/(MS) and p is the integer portion of n/(MS); and

quantizing each sum to the one or more quantized bits of each selected data sample.

25. (Original) A device for processing a sampled DS-CDMA signal as in claim 23, wherein the n^{th} element of said data sequence is denoted by c(n), wherein said sampled DS-CDMA signal includes a training sequence and wherein said coherently averaging comprises:

calculating the sums $\sum_{p=0}^{P-1} c(k + M \cdot S \cdot p) pn(k, b(p))$, where P is the number of averages, S is the number of samples per chip, M is the number of chips per information bit, k is the remainder portion of n/(MS), p is the integer portion of n/(MS), b(p) is the value of the p^{th} bit in the training sequence and pn(k,b(p)) is the value of the k^{th} chip of the pseudo-noise code for the bit b(p); and

quantizing each sum to the one or more quantized bits of each selected data sample.

26. (Original) A device for processing a sampled DS-CDMA signal as in claim 23, wherein said correlating said averaged data sequence with a pseudo-noise code comprises:

storing said averaged data sequence as a data bit pattern;

storing said pseudo-noise sequence as a pseudo-noise bit pattern;

performing a bit-wise "exclusive-or" operation between said data bit pattern and said pseudo-noise bit pattern;

calculating from the result of said "exclusive-or" operation the number of bits that match between said data bit pattern and said pseudo-noise bit pattern.